Advanced Metallization Conference (AMC) 2009

October 13-15, 2009
Baltimore, Maryland

FINAL PROGRAM

Tuesday, October 13

8:30-8:40 Welcome and opening remarks
Stefan Schulz and Dan Edelstein

8:40-9:25 **Keynote address:** Commercialization of 'Ink Based' and Low Cost CIGS Solar Cells/Modules
Vijay Kapur, International Solar Electric Technology, Inc.

Session IA: Barrier/Seed (IA)

Session Chairs: Mehul Naik and John Ekerdt

9:25-9:55 **IA.1 Invited**: Extendibility of PVD Barrier and Seed Processes
Prabu Gopalraja, AMAT

9:55-10:25 **IA.2 Invited:** Copper Films Grown via Copper Oxide ALD: Routes and Challenges for Integration with Next-Generation Interconnect Materials
Thomas Wächtler, Chemnitz University of Technology

10:25-10:45 ***Break***

10:45-11:05 **IA.4** Thin MnO Barrier Formation with CVD for Copper Contact Plug on Nickel Silicide
K. Neishi, T. Sagawa, Y. Sutou and J. Koike
Dept. of Materials Science, Tohoku University
Japan

Session IB: Metallization (IB)

Session Chairs: Heinrich Korner and Andrew McKerrow

11:05-11:25 **IB.1** A study on Resistivity Increase of Copper Interconnects with the Dimension Comparable to Electron Mean Free Path Utilizing Monte Carlo Simulations
Makoto Wada, Takashi Kurusu, Yosuke Akimoto, Noriaki Matsunaga, Hiroyoshi Tanimoto, Nobutoshi Aoki, Yoshiaki Toyoshima and Hideki Shibata
Center for Semiconductor Research and Development, Semiconductor Company, Toshiba Corporation
Japan

11:25-11:45 **IB.2** Tungsten Contact and Line Resistance Reduction with Advanced Pulsed Nucleation Layer (PNL) and Low Resistivity Tungsten (LRW) Treatment
Anand Chandrashekar[a†], Feng Chen[a], Jasmine Lin[a], Raashina Humayun[a], Panya Wongsenakhum[a], Sean Chang[a], Michal Danek[a], Erich Klawuhn[a], Takamasa Itou[b], Tomoo Nakayama[b], Atsushi Kariya[b], Masazumi Kawaguchi[c], Shunichi Hizume[c]

[a]Direct Metals Business Unit, Novellus Systems, Inc., San Jose, CA, USA
[b]NEC Electronics Corporation, Japan
[c]Novellus Systems Japan, Japan

11:45-12:05 **IB.3** Quantitative Analysis of The Impact of Surface And Grain Boundary Scattering on the Resistivity of Nanometric Cu films
Tik Sun[1], Bo Yao[1], Andrew P. Warren[1], Katayun Barmak[2], Michael F. Toney[3], Robert E. Peale[4], and Kevin R. Coffey[1, 4]*
[1]*Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando FL*
[2]*Department of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA*
[3]*Stanford Synchrotron Radiation Lightsource, Menlo Park, CA*
[4]*Department of Physics, University of Central Florida, Orlando, FL*

12:05-13:00 ***Lunch***

13:00-13:10 ***Housekeeping***

Session II: Low-k Dielectrics (II)

13:10-13:40 **II.1 Invited**: Characterization Methods of Copper Low-k Interconnects
T. Nakamura, Fujitsu

13:40-14:00 **II.2** Silicon Precursor Development for Advanced Barrier Integration
Laura Matz[*], Anupama Mallikarjunan, Raymond N. Vrtis, Andrew D. Johnson, Shawn Jiang, Mark L. O'Neill
[1]*Air Products and Chemicals, Inc., Allentown, PA*

14:00- 14:20 **II.3** Restoration of Plasma Damaged Porous Ultra Low-k SiOCH Films: A Coating Process with UV Activation Versus a Vapor Phase Process with Thermal Activation
T. Oszinda[1], M. Schaller[2], D. Fischer[2], S. Leppack[2] and S. E. Schulz[3]
[1]*Fraunhofer CNT, Dresden, Germany*
[2]*GLOBALFOUNDRIES Dresden Module Two GmbH & Co KG, Germany*
[3]*TU Chemnitz/Fraunhofer ENAS, Chemnitz, Germany*

14:20-14:40 **II.4** Dielectric Recovery of Plasma Damaged Organosilicate Low-k Films by UV and Silylation Treatments
H. Huang [a)], H. Shi, J. Bao, J. Im, P. S. Ho
Laboratory for Interconnect and Packaging, Microelectronics Research Center, The University of Texas at Austin, Austin, TX
M. L. McSwiney, M. D. Goodner, M. Moinpour, and G. M. Kloster
Intel Corporation, Logic Technology Development, Hillsboro, OR, U.S.A
Y. Zhou, J. T. Pender, M. Armacost, D. Kyser
Applied Materials, Sunnyvale, CA

14:40-15:00 **II.5** Porogen Residue Free Ultra Low-k PECVD Material: Fabrication, Optical and Mechanical Properties
A.M. Urbanowicz[1, a], K. Vanstreels, P. Verdonck, D. Shamiryan, M. Cremel[2], S. De Gendt[1] and M.R. Baklanov
IMEC, Heverlee, Belgium
[1]*also at Dept. Chem, Katholieke Univ Leuven, Heverlee, Belgium*
[2]*also at Dept. Mat. Eng., INSA de Lyon, Villeurbanne, France*

15:00-15:20 ***Break***

15:20-15:40 **II.6** A Path to Successful Integration of Porous Dielectrics in the BEOL
S. Gates[*], A. Grill, S.-T. Chen[1], T. Spooner[1], E. Todd Ryan[2], S. Papa Rao, M. Krishnan, G. Dubois[3], D. Canaperi[1], S. Cohen, Y. Ostrovski

IBM T.J. Watson Research Center, Yorktown Hts. NY, USA
[1]IBM at Albany Nanotech, Albany NY, USA
[2]GLOBALFOUNDRIES, Inc. at Albany Nanotech, Albany NY, USA
[3]IBM Almaden Research Center, San Jose CA, USA

Session IIIA: Integration

Session Chairs: Jan Chia-Hong and Stephen Russell

15:40-16:10 **IIIA.2 Invited:** Key Aspects of CoWP and ULK Implementation into High-Volume Manufacturing for Future Technologies
M. Nopper

16:10-16:30 **IIIA.1** Advanced Metallization Developments for 32-nm node CMOS Technology Contact Architecture
Doug H. Lee, Valli Arunachalam, Filippos Papadatos[1], Hao Zhang[2], Zhengwen Li[1], Keith Wong[1], Woo-Hyeong Lee[1], Shurong Liang, Michael Chudzik[1], David Brown, Dan Mocuta[1], Doug Bonser, John Pellerin
GLOBALFOUNDRIES, Inc., [1]IBM Systems & Technology Group, [2]Chartered Semiconductors at IBM Semiconductor Research & Development Center (SRDC), Hopewell Junction NY, USA

16:30-16:50 **IIIA.6** Integration of an Organic Ultra Low-k (k=2.2) Material
M. Pantouvaki, L. Zhao[*], C. Huffman, N. Heylen, A. Ferchichi, Y. Ono[**], M. Nakajima[**], K. Nakatani[**], H. Struyf, G. P. Beyer and M. R. Baklanov
IMEC, Leuven, Belgium
[*]Intel Corporation, Leuven, Belgium
[**]Sumitomo Bakelite Co., Ltd., Japan

17:30-20:00 **POSTER SESSION**

Wednesday, October 14

Session IIIA: Integration (continued)

Session Chairs: Jan Chia-Hong and Stephen Russell

8:30-8:50 **IIIA.3** CoWP Metal Caps for Reliable 32 nm 1X Cu Interconnects in Porous ULK (k=2.4)
E. Huang[1], M. Oh[3], S. B. Law[4], S. Petitdidier[5], T.-M. Ko[2], H. Sawada[6], T. J. Tang[4], C.-K. Hu[1], S. Cohen[1], E. Liniger[1], G. Bonilla[1], D. Rath[1], T. Shaw[1], L. Gignac[1], D. Edelstein[1], D. Permana[3], C. Child[3], R. Buengener[3], J. Fitzsimmons[2], P. Findeis[2], C. Taft[2], M. Angyal[2], O. Ogunsola[2], J. King[2], P. Flaitz[2], F. Baumann[2], S. Molis[2], C. Dziobkowski[2], J. Coffin[2], R. Davis[2], M. Zaitz[2], A. Kapur[2], L. Kermel[2], C. Truong[2], S. Grunow[2], X. Chen[2], M. Sankarapandian[2] , B. Li[7], F. Chen[7], T. Lee[7], C. Christiansen[7], A. Kolics[8], N. Gilbert[8], O. Rigoutat[8], and N. Li[8]
[1]IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA;
[2]IBM Microelectronics Division
[3]GLOBALFOUNDRIES, Inc.
[4]Chartered Semiconductor Manufacturing
[5]STMicroelectronics
[6]Toshiba America Inc.,Hopewell Junction, NY, USA
[7]IBM Burlington, Essex Junction, VT 05452, USA;
[8]Lam Research Corporation, Fremont, CA, USA

8:50-9:10 **IIIA.4** Performance of Cu dual-Damascene Interconnects Using a Thin Ti-Based Self-Formed Barrier Layer for 28-nm Node and Beyond

°*Kazuyuki Ohmori[1], Kenichi Mori[1], Kazuyoshi Maekawa[1], Kazuyuki Kohama[2], Kazuhiro Ito[2], Takashi Ohnishi[4], Masao Mizuno[5], Koyu Asai[1], Masanori Murakami[3] and Hiroshi Miyatake[1]*
[1]Renesas Technology Corp., 4-1, Mizuhara, Itami, Hyogo, 664-0005, Japan
[2]Dept. of Materials Science and Engineering, Kyoto Univ., Yoshida-Honmachi, Sakyo-ku, 606-8501 Kyoto, Japan
[3]The Ritsumeikan Trust, Nakagyo-ku, 604-8520 Kyoto, Japan
[4]KOBE STEEL,LTD, Materials Research Laboratory Surface Design & Corrosion Research Section
[5]KOBE STEEL,LTD, Electronics Research Laboratory, Thin Film Section

9:10-9:30 **IIIA.5** UV Curing-Induced Photoresist Poisoning in Advanced ULK BEOL Integration Schemes
[1]Y. C. Ee, [2]D. Kioussis, [3]M.S Angyal, [3]A. Kapur, [3]Y. Feng, [3]A. Passano, [3]N. Klymko, [3]A. Madan, [3]J.L. Wang, [3]J.A Fitzsimmons, [3]S.Y. Chong, [2]D. Permana, [3]O.O Ogunsola, [2]C. Child, [3]T-J. Cheng, [1]Z. G. Sun, [3]Y. J. Choi, [3]H. Yusuff, [3]S.A Sieg, [2]J. Linville, [3]S. Grunow, [3]G. Biery*
IBM Semiconductor Research and Development Center (SRDC), Hopewell Junction NY
[1]Chartered Semiconductor Manufacturing
[2]GLOBALFOUNDRIES, Inc.
[3]IBM Microelectronics

Session IIIB: Reliability & Yield

Session Chairs: Cindy Goldberg and Zsolt Tokei

9:30-10:00 **IIIB.1 Invited:** Cu BEOL Reliability
Tony Oates

10:00-10:30 **IIIB.6 Invited**: Statistical Aware Design for sub-nm Technology/Design
Rajiv Joshi

10:30-10:50 ***Break***

10:50-11:10 **IIIB.2** Electromigration Improvement for 40 nm and Below through Diffusion Barrier Interface Engineering Using New Precursor
L.Q. Xia

11:10-11:30 **IIIB.3** Adhesion, Cu Voiding, and Debonding Kinetics of Copper / Dielectric Diffusion Barrier Films
*Ryan Birringer[*1], Roey Shaviv[2], Tom Mountsier[2], Jon Reid[2], Jian Zhou[2], Roy H. Geiss[3], David Read[3], and Reinhold Dauskardt[1]*
[1)]Department of Materials Science and Engineering, Stanford University, Stanford, CA
[2)]Novellus Systems Inc., San Jose, CA
[3)]National Institute of Standards, Boulder, CO

11:30-11:50 **IIIB.4** Ageing Failure of Power MOSFET Metallization Studied by Electron and Ion Microscopy
D. Martineau[a], T. Mazeaud[b], M. Legros[a], Ph. Dupuy[b], C. Levade[a,c], G. Vanderschaeve[a,c]
[a]CEMES-CNRS, Cedex 4
[b]Freescale Semiconductors, Toulouse
[c]Université de Toulouse, INSA, Cedex

11:50-12:10 **IIIB.5** Impact of Impedance Mismatch of on-die Interconnects and Logic Cells on Device Reliability and Functionality
[*]Pavel Livshits[1], M. Gurfinkel[2], A. Rysin[2,3], S. Sofer[3], Y. Shapira[2] and Y. Fefer[3]
[1]Engineering School, Bar Ilan University, Israel
[2]School of Electrical Engineering, Tel Aviv University, Tel Aviv, Israel

[3]Freescale Semiconductor Israel Ltd., Herzlia, Israel

12:10-13:10 ***Lunch***

13:10-13:20 ***Housekeeping***

Session IV: 3D Integration

13:20-13:50 **IV.1 Invited:** Metal Integration Strategies for 3D
Patrick Leduc
Through Silicon via Integration Strategy for 3D

13:50-14:20 **IV.2 Invited**: Si Carrier for Heterogeneous 2-D and 3-D Integration
John Knickerbocker

14:20-14:50 **IV.3 Invited** :TSV Capacitance modelling
Saibal Mukhopadhyay

14:50-15:10 ***Break***

15:10-15:40 **IV.4 Invited**: Characterization of High-Speed Digital and RF Interconnect-Chip-Package Systems Including Stacked Chip and 3-D Packages
William Eisenstadt

15:40-16:00 **IV.5** CMOS Compatible Insulated Through Silicon Vias for 3D Silicon
A. K. Stamper[4], M. Shapiro[1], R. Herrin[4], V. Carlos[4], E. White[4], M. Brigham[4], B. Porth[4], J. Levy[4], D. Dang[4], A. Gupta[4], M. Interrante[2], P. Andry[3], B. Dang[3], C. Tsang[3], R. Liptak[2], J. Griffith[2], E. Sprogis[4], L. Guerin[5], V. Truong[5], D. Berger[2] and J. Knickerbocker[3]
[1]IBM Microelectronics, Austin, TX
[2]IBM Microelectronics, Hopewell Junction, NY
[3]IBM Research, Yorktown Heights, NY
[4]IBM Microelectronics, Essex Junction VT
[5]IBM Canada, Bromont QC

16:00-16:20 **IV.6** Electrochemical Deposition of Reactive Nanoscale Metallization Systems for Low Temperature Bonding in 3D Integration
L. Hofmann[1], J. Braeuer[2], M. Baum[2], S. E. Schulz[2], T. Gessner[1, 2]*
[1]Chemnitz University of Technology, Center for Microtechnologies, Chemnitz. Germany
[2]Fraunhofer ENAS Chemnitz, Chemnitz, Germany

16:20-16:40 **ADMETA PREVIEW**
Yukihiro Shimogaki
The University of Tokyo

17:30-20:00 **Special Event ---- Location TBA**

Thursday, October 15

Session V: Emerging Applications

8:30-9:00 **V.1 Invited:** Advanced Characterization of Integrated Nano Materials
Sylvain Maitrejean

9:00-9:30 **V.2 Invited:** Resistive Switching Memories
Christoph Muller

9:30-9:50 **V.3:** MEMS Indicator Configurations with Chields for Achieving Large Inductance Variations
Yutaka Mizuochi, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu
Integrated Research Institute, Tokyo Institute of Technology
Japan

9:50-10:20 **V.4: Invited:** Metallization Challenges in Solar Cell; e.g. Highly Efficient Back Contact Solar Cells
Emmanuael Van Kerschaver

10:20-10:40 **Break**

Session VI: Patterning, CMP, and Cleaning

10:40-11:10 **VI.1 Invited:** Metal Hard-Mask Based Souble Patterning for 22nm and Beyond
Herbert Struyf

11:10-11:30 **VI.2** Investigation of Cu Bimetallic Corrosion in CMP Chemical Environments using Micropattern Corrosion Screening
Praveen R. Nalla, Kyle K. Yu, Karthikeyan S.M. Pillai, Oliver Chyan[*]
Departments of Chemistry, Materials Science and Engineering
University of North Texas
Denton, Texas TX 76203

11:30-11:50 **VI.3** Modeling and Applications of Copper Interconnect Chemical Mechanical Polishing (CMP) Simulation
Senthil Arthanari, Marci Liao, Shia Yu, Anand Inani, Katsuhiro Shimazu, Brian Stine
PDF Solutions, Inc. San Jose, CA

11:50-12:10 **VI.4** Improvement of Etch Processes for SiCOH Materials with Novel *in situ* Diagnostic and Evaluation Methods
S. Zimmermann[1,], N. Ahner[1], F. Blaschta[1], M. Schaller[2], H. Zimmermann[3], H. Rülke[2], N. Lang[3], J. Röpcke[3], S.E. Schulz[1,4], T. Gessner[1,4]*
[1)]Fraunhofer ENAS, Chemnitz, Germany
[2)]Globalfoundries Dresden Module Two GmbH & Co. KG,Dresden, Germany
[3)]INP Greifswald e.V., Greifswald, Germany
[4)]Chemnitz University of Technology, Center for Microtechnologies, Chemnitz, Germany

12:10-12:30 **VI.5** Amorphous Carbon Hard Mask for 45nm Contact Patterning
X.S. Rao[1], J. Widodo[1], W. Lu[1], M.S. Zhou[1], L.C. Hsia[1],*
T. Chu[2], R.K.H. Lee[2], A. Jain[2], H. Yu[2], B.T. Nguyen[2], and D. Padhi[2]
[1]Chartered Semiconductor Manufacturing. Ltd., Singapore
[2]Applied Materials South East Asia. Singapore

12:30-12:50 **VI.6** The Effect of Plating and Anneal Conditions on Post CMP Defects
Marcelle Marshall, Roey Shaviv, Tom Mountsier, Jon Reid, Andrew McKerrow
Novellus Systems Inc. San Jose CA

12:50-13:00 **Closing Remarks**

13:00-14:00 ***Lunch***

POSTER SESSION

P.I. Metallization

Session Chairs: John Ekerdt and Heinrich Korner

P.I.1 Origins of Large Variation in Ductility of Thin Nanocrystalline Metallization on Polymer Substrates

*Teng Li[1, 2, *], Zhao Zhang[1], Benoit Michaux[1]*
[1]Department of Mechanical Engineering, University of Maryland, College Park, MD
[2]Maryland NanoCenter, University of Maryland, College Park, MD

P.I.2 Nucleation Effects of Tungsten Chemical Vapor Deposition on B2H6 Pre-Treated Titanium Nitride for sub-45 nm Contacts

*A. Rozenblat[1 *], R. Drori[1], Y. Shacham-Diamand[2] and D. Horvitz[1]*
[1]Numonyx Israel ltd., Israel
[2]Electrical Engineering, Tel Aviv University, Tel Aviv, Israel.

P.I.3 The Step Coverage Quality of Cu film by SCFD Compared with CVD

Takeshi Momose, Masakazu Sugiyama, and Yukihiro Shimogaki*
Department of Materials Engineering, The University of Tokyo
** Institute of Engineering Innovation, The University of Tokyo*
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

P.I.4 Evaluation of Selective Metal Deposition (Selectroplating®)

Rashid Mavliev
IPGRIP LLC., 502 E. John St., NV, 89706

P.II Low-k Dielectrics

Session Chairs: Zsolt Tokei and Roey Shaviv

P.II.1 Penetration Characteristics of ALD-TiN to 1 nm-pore Low-k SOD Films

°M. Hirakawa, T. Yamazaki, I. Tojo, T. Nakayama and H. Murakami
Tsukuba Institute for Super Materials in Susono Section, ULVAC, Inc. 1220-1 Suyama, Susono, Shizuoka, 410-1231, Japan

P.II.2 UV assisted curing of plasma damaged porous ultralow-k materials for a k-recovery process: influence of curing-cycle modifications

[*]N Ahner[1], T. Fischer[2], S. Zimmermann[1], M. Schaller[3], L. Prager[4], S.E. Schulz[1]
[1]Fraunhofer ENAS, Chemnitz, Germany
[2]Chemnitz University of Technology, Chemnitz, Germany
[3]Globalfoundries Inc., Dresden, Germany

P.III Materials & Characterization

Session Chairs: Reinhold Dauskardt and Paul-Henri Haumesser

P.III.1 Electronic Transport Properties of Copper Atomic Wires

*Saeideh Mohammadzadeh[1, *], Reinhard Streiter[1, 2], and Thomas Gessner[1, 2]*
[1]Center for Microtechnologies, ZFM, Chemnitz University of Technology, Chemnitz, Germany
[2]Fraunhofer Research Institute for Electronic Nano Systems, ENAS, Chemnitz, Germany

P.III.2 Low temperature silicidation of Pd layers on crystalline silicon monitored via in situ resistance measurements

E. J. Faber[1], R.A.M. Wolters[1,2], B. Rajasekharan[1], C. Salm[1], J.Schmitz[1]*
[1]MESA+ Institute for Nanotechnology, University of Twente, Semiconductor Components Group, The Netherlands
[2]NXP research, Eindhoven, The Netherlands

P.III.3 Characterization of Carbon States in ULK Porous Films

M.K. Haas[1], L. –S Du, R.N. Vrtis, S.J. Weigel, P.L. McDaniel, K.E. Theodorou, L. M. Matz, M.L. O'Neill
Air Products and Chemicals Inc, Allentown PA

P.III.4 Determinant of Electrical Leakage Current for porous SiOC Film
Kiyohiro Matsushita, Akinori Nakano, Ippei Yanagisawa, Yuya Nonaka, and Nobuyoshi Kobayashi
ASM Japan K.K., Tokyo, Japan

P.III.5 Effects of Fluorine Species on Suppressing Ni(Pt) Salicide Defects
Jerander Laia, Yi-Wei Chenb, Nien-Ting Hoc, T.C. Tsaid, C.C. Huange, and J.Y. Wu
UMC, Taiwan, R.O.C.

P.III.6 Evolution of Cu/ SiO2 and Cu/Ta Interface Roughness with Annealing
Andrew P. Warren[1], Tik Sun[1], Bo Yao[1],Katayun Barmak[2], Michael F. Toney[3], and Kevin R. Coffey[1]*
[1]Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando FL
[2]Department of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA
[3]Stanford Synchrotron Radiation Laboratory, Menlo Park, CA

P.IV Integration

Session Chairs: Andrew McKerrow and Chia-Hong Jan

P.IV.I Seed Layer Enhancement: An Efficient Process for the Fabrication of 3D Interconnects
J.Cuzzocrea[1], E. Deronzier[2], P.H. Haumesser[2], M. Assous[2], J.B. De Labretoigne[3], R. Baskaran[3], E. Chaînet[4]
[1]STMicroelectronics, Grenoble, France
[2]CEA- LETI – MINATEC –Grenoble – France
[3]SEMITOOL, Grenoble, France
[4]LEPMI, UMR Cedex, France

P.IV.2 Electroless CoWP Integration Scheme to Enhance Cu Interconnect Reliability at Ultra Narrow Line
Kwang-Jin Moon, Jong-Ho Yun, Zung-Sun Choi, Hye-Kyung Jung, Jong-Myeong Lee, Gil-Heyun Choi, Siyoung Choi, Joo-Tae Moon*
Process Development Team, Semiconductor R&D Center, Samsung Electronics, Korea

P.V 3-D Integration

Session Chairs: Steve Russell and Peter Ramm

P.V.1 Seed Layer Enhancement: An Efficient Process for the Fabrication of 3D Interconnects
J.Cuzzocrea[1], E. Deronzier[2], P.H. Haumesser[2], M. Assous[2], J.B. De Labretoigne[3], R. Baskaran[3], E. Chaînet[4]
[1]STMicroelectronics, Grenoble, France
[2]CEA- LETI – MINATEC –Grenoble – France
[3]SEMITOOL, Grenoble, France
[4]LEPMI, UMR Cedex, France

P.V.2 Development of Permanent Bonding Material for 3DI Process
°Hiroyuki Uehara[1], Junko Katayama[1], Koji Fujimoto[2], Nobuhide Maeda[3], Hideki Kitada[3],
Kosuke Suzuki[2], and Takayuki Ohba[3]
[1]Nissan Chemical Industries, Ltd.
[2]Dai Nippon Printing
[3]The University of Tokyo

P.V.3 Challenges of Thermo-Mechanical Reliability in 3-D Integration with TSVs

Xuefeng Zhang, Kuan H. Lu, Suk-Kyu Ryu, Jay Im, Rui Huang*, and Paul S. Ho*
Microelectronics Research Center, The University of Texas at Austin, USA
Aerospace Engineering and Engineering Mechanics Department, The University of Texas at Austin, USA

P.V.4 Application of Self Assembly Monolayer (SAM) in Cu-Cu Bonding Enhancement at Low Temperature for 3-D Integration
*Dau Fatt Lim, Shiv Govind Singh, Jun Wei[1], Chee Mang Ng[2], and Chuan Seng Tan**
School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
[1]SIMTech, Singapore; 2 Chartered Semiconductor Manufacturing Company, Singapore

P.V.5 Influence of Different Additive Systems on TSV Cu plating
Albrecht Uhlig, Dirk Rohde, Thomas Dretschkow, Thomas Beck
Atotech Deutschland GmbH; Berlin; Germany

P.V.6 Wafer Level Alignment Accompanied With Wafer Stacking for Wafer-on-a-Wafer (WOW) Technology Using Polymer Adhesive
°Miyuki Akazawa[1], Koji Fujimoto[1], Hiroyuki Uehara[2], Junko Katayama[2] , Nobuhide Maeda[3], Hideki Kitada[3], Kosuke Suzuki[1], and Takayuki Ohba[3]
[1]Dai Nippon Printing
[2]Nissan Chemical Industries, LTD.
[3]The University of Tokyo

P.VI Emerging Applications

Session Chairs: Yosi Shacham-Diamond and Rajiv Joshi

P.VI.1 Metallic Conduction in ZnO/Cu/ZnO Thin Films
K. Sivaramakrishnan and T. L. Alford
School of Materials and Flexible Display Center at ASU
Arizona State University, Tempe, Arizona

P.VI.2 Effect of Thermal Processing on Silver Contacts for Zinc Oxide and Indium Tin Oxide
K. Sivaramakrishnan[1], A. T. Ngo[1], S. Iyer[2], and T. L. Alford[1]
[1]School of Materials and Flexible Display Center at ASU, Arizona State University, Tempe, Arizona
[2]Department of Electrical and Computer Engineering, North Carolina Agricultural and Technical State University, Greensboro, NC

P.VII Patterns & CMP Cleaning

Session Chairs: Cindy Goldberg and Mehul Naik

P.VII.1 Impact of Different Acidic Treatments on Aluminum During the Clean Step
S. Bilouk[1, 2], L. Broussous[1], R P. Nogueira[2], C. Jayet[3], C. Pernel[3]*
[1]STMicroelectronics, Centre de Recherche Crolles, Cedex, France
[2]UMR St. Martin d'Hères, France
[3]CEA-LETI, France